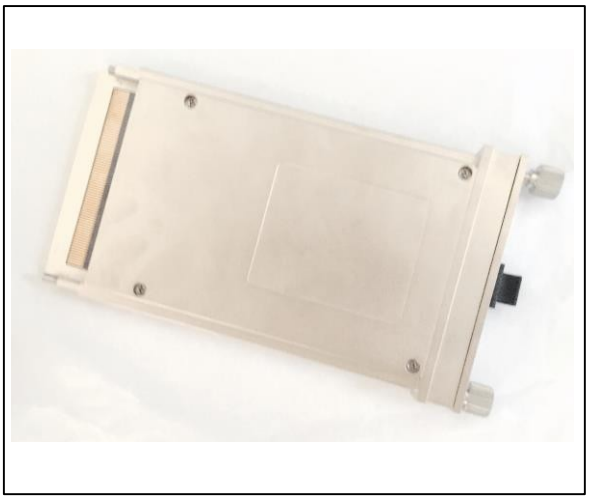
100Gb/s 850nm 10x 10.3G CFP SR10 TRx, 100m
HOLS-CFP85M1-M5D-CV

Features



- ☑ Integrated 10 independent full duplex channels
- ☑ Transmission distance up to 100m (MM fiber)
- ☑ Support CFP MSA and CAUI electrical interface
- ☑ Compliant to IEEE 802.3ba 100Gbase-SR10
- ☑ Control functions through the CFP management interface
- ☑ CFP Power Class 1 (<8W)
- ☑ RoHS 6/6 compliant

Description

The transceiver is a hot pluggable fiber optic transceiver in the CFP form factor. Integrating 10 independent channels of 10G transmitting and receiving functions makes it ideally suited for 100G very short reach applications where cost effective high bandwidth is needed. The diagnostic and control functions are integrated into the design via a set of non-data hardware signal pins and Management Date Input/Output (MDIO) interface per the CFP Multi-Source Agreement (MSA) Management Interface Specification draft 1.4.

The transceiver supports an aggregate bandwidth of 100G over 100 meters of optical fiber. Each lane transmits and receives data streams at typical data rate of 10.3125Gbps. The CFP transceiver has a single MPO port which connects to an industry standard 2x12 multi-mode fiber cable. It provides an excellent solution for 100GbE data transmission at 850nm over up to 100m multimode mode ribbon cables. The product is designed and tested in accordance with industry safety standards. The transceiver is Class 1 Laser product per U.S. FDA/CDRH and international IEC-60825 standards.

The transceiver connects to standard 148-pin CFP connectors for hot plug capability. This allows the system designer to make configuration changes or maintenance by simply plugging in different transceivers without removing the power supply from the host system. The transmitter and receiver DATA interfaces are internally AC-coupled. LV-CMOS Transmitter Disable control input and Loss of Signal (LOS) output interfaces are also provided.

The transceiver can be conveniently assembled into and released from the host system through the railing system specified in the CFP MSA.

The transceiver operates from a single +3.3V power supply over an operating case temperature range of 0℃ to +70℃. The housing is made of metal for EMI immunity.

Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
Storage Temperature Range	T_{ST}	- 40	+ 85	°C
Case Operating Temperature	T_{OP}	0	+ 70	°C
Operating Relative Humidity[1]	*RH*	5	95	%
Supply Voltage Range	V_{CC}	- 0.3	+ 4	V
Input LVTTL and LVCMOS signals	-	0	+ 3.6	V
[1]Non condensing				

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Transmitter Performance Characteristics (Over Operating Case Temperature Range, V_{CC}=3.2 to 3.4V)

Parameter	Symbol	Min	Typ	Max	Units
Signaling speed (per lane)	*B*	-	10.3125	-	Gb/s
Lane wavelengths	λ	840	850	860	nm
Spectral width	$\Delta\lambda_{rms}$	-	0.5	0.65	nm
Average launch power[1] (per lane)	P_{avg}	- 8	- 2.5	+ 1	dBm
Optical modulation amplitude (per lane)	P_{OMA}	- 6	-	+ 3	dBm
Extinction ratio	*ER*	3	-	-	dB
Optical return loss tolerance	-	-	-	12	dB
Average launch power of OFF transmitter	P_{off}	-	-	- 30	dBm
Transmitter and dispersion penalty	*TDP*	-	-	3.0	dB
Optical output eye	Compliant with IEEE802.3ba				

[1]Average power figures are informative only

Note: The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature. The Rx parameters are measured at TP3 as defined in IEEE 802.3ba.

Receiver Performance Characteristics (Over Operating Case Temperature Range, V_{CC}=3.2 to 3.4V)

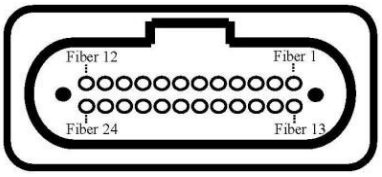
Parameter		Symbol	Min	Typ	Max	Units
Signaling speed (per lane)		*B*	-	10.3125	-	Gb/s
Wavelength of operation		λ	840	850	860	nm
Overload		-	+ 1	-	-	dBm
Stressed sensitivity in OMA (per lane)[2]		-	-	-	- 5.4	dBm
Optical return loss		-	12	-	-	dB
LOS hysteresis		-	0.5	-	-	dB
LOS thresholds[3]	Increasing light input	P_{los+}	-	-	- 10	dBm
	Decreasing light input	P_{los-}	- 30	-	-	

[1]Average receive power is informative only
[2]Measured with conformance test signal as specified in IEEE 802.3ba

Note: The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature. The Rx parameters are measured at TP3 as defined in IEEE 802.3ba.

CFP Optical Interface Lanes and Assignment

Below figure and table shows the multimode fiber facets of the optical connector and lane assignment.



Fiber #	Lane Assignment	Corresponding Electrical pins		Fiber #	Lane Assignment	Corresponding Electrical pins
1	Unused			13	Unused	
2	RX0	79,80		14	TX0	113,114
3	RX1	82,83		15	TX1	116,117
4	RX2	85,86		16	TX2	119,120
5	RX3	88,89		17	TX3	122,123
6	RX4	91,92		18	TX4	125,126
7	RX5	94,95		19	TX5	128,129
8	RX6	97,98		20	TX6	131,132
9	RX7	100,101		21	TX7	134,135
10	RX8	103,104		22	TX8	137,138
11	RX9	106,107		23	TX9	140,141
12	Unused			24	Unused	

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Transmitter Electrical Characteristics (Over Operating Case Temperature range, V_{CC}=3.2 to 3.4V)

Parameter	Symbol	Min	Typ	Max	Units
Differential input impedance	Z_d	-	100	-	Ω
Differential input voltage swing	$V_{PP-DIFF}$	20		1600	mV
Input high voltage	V_{IH}	2.0	-	V_{cc}	V
Input low voltage	V_{IL}	0	-	0.7	V

Receiver Electrical Characteristics (Over Operating Case Temperature range, V_{CC}=3.2 to 3.4V)

Parameter	Symbol	Min	Typ	Max	Units
Differential output impedance	Z_d	-	100	-	Ω
Differential output swing	$V_{PP-DIFF}$	-	600	800	mV
Output rise and fall time (20% to 80%)	t_{RH}, t_{FH}	-	-	35	ps
Inter-channel skew	-	-	-	150	ps
Signal detect assert timing	-	-	100	-	μs
Signal detect de-assert timing	-	-	100	-	μs

Electrical Power Supply Characteristics (Over Operating Case Temperature range, V_{CC}=3.2 to 3.4V)

Parameter		Symbol	Min	Typ	Max	Units
Power supply voltage		V_{CC}	3.13	3.3	3.47	V
Power consumption in operating condition		P_W	-	6.1	8	W
Inrush current		-	-	-	50	mA/μs
Turn-off current		-	-50	-	-	mA/μs
Power supply noise	DC – 1MHz	V_{rip}	-	-	2	%
	1 – 10MHz		-	-	3	

Laser Safety:

All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825 standards. They must be operated under specified operating conditions.

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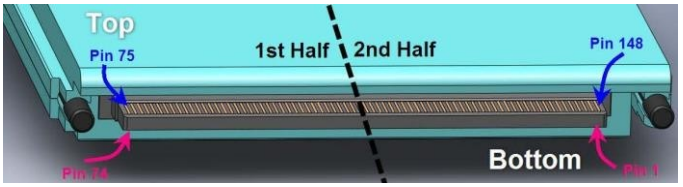
Connector Pin-out



Electrical Pin Definition

Pin	Logic	Symbol		Name/De
1-5	GND	*3.3V_GND*	3.3V Module Supply Voltage Return Ground	
6-15	Vcc	*3.3V*	3.3V Module Supply	
16-20	GND	*3.3V_GND*	3.3V Module Supply Voltage Return Ground	
21-22	-	*DNC*	Module Vendor I/O. Do not connect	
23	GND	*GND*	Ground	
24	CML	*TX_MCLKn*	Not used	
25	CML	*TX_MCLKp*	Not used	
26	GND	*GND*	Ground	
27-29	-	*DNC*	Module Vendor I/O. Do not connect.	
30	LVCMOS w/ PU	*PRG_CNTL1*	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn – TX & RX IC reset. “0” = reset, “1” or NC = enabled or not used	
31	LVCMOS w/ PU	*PRG_CNTL2*	Programmable Control 2 set via MDIO, MSA default: Hardware power Interlock LSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used	
32	LVCMOS w/ PU	*PRG_CNTL3*	Programmable Control 3 set via MDIO, MSA default: Hardware power Interlock MSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used	
33	LVCMOS	*PRG_ALRM1*	Programmable Alarm 1 set via MDIO, MSA default: RXS, RX CDR Lock Indicator, “1” = loss of lock, “0” = locked	
34	LVCMOS	*PRG_ALRM2*	Programmable Alarm 2 set via MDIO, MSA default: HIPWR_ON, “1” = module power up completed, “0” = module not powered up	
35	LVCMOS	*PRG_ALRM3*	Programmable Alarm 3 set via MDIO, MSA default: MOD_READY, module initialization done, “1” = complete, “0” = not done	
36	LVCMOS w/ PU	*TX_DIS*	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled	
37	LVCMOS w/ PU	*MOD_LOPWR*	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled	
38	GND	*MOD_ABS*	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host	
39	LVCMOS w/ PD	*MOD_RSTn*	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull Down resistor in module	
40	LVCMOS	*RX_LOS*	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition	
41	LVCMOS	*GLB_ALRMn*	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm	
42	1.2V CMOS	*PRTADR4*	MDIO port address bit 4	
43	1.2V CMOS	*PRTADR3*	MDIO port address bit 3	
44	1.2V CMOS	*PRTADR2*	MDIO port address bit 2	
45	1.2V CMOS	*PRTADR1*	MDIO port address bit 1	
46	1.2V CMOS	*PRTADR0*	MDIO port address bit 0	
47	1.2V CMOS	*MDIO*	Management Data I/O bi-directional data (electrical specs as per 802.3ae)	
48	1.2V CMOS	*MDC*	Management data clock (electrical specs as per 802.3ae)	

49	GND	*GND*	Ground
50-51	-	*DNC*	Module Vendor I/O. Do not connect.
52	GND	*GND*	Ground
53-54	-	*DNC*	Module Vendor I/O. Do not connect.
55-59	GND	*3.3V_GND*	3.3V Module Supply Voltage Return Ground
60-69	Vcc	*3.3V*	3.3V Module Supply
70-74	GND	*3.3V_GND*	3.3V Module Supply Voltage Return Ground
75	GND	*GND*	Ground
76	CML	RX_MCLKp	Not used
77	CML	RX_MCLKn	Not used
78	GND	*GND*	Ground
79	CML	*RX0p*	High speed receiver data
80	CML	*RX0n*	High speed receiver data
81	GND	*GND*	Ground
82	CML	*RX1p*	High speed receiver data
83	CML	*RX1n*	High speed receiver data
84	GND	*GND*	Ground
85	CML	*RX2p*	High speed receiver data
86	CML	*RX2n*	High speed receiver data
87	GND	*GND*	Ground
88	CML	*RX3p*	High speed receiver data
89	CML	*RX3n*	High speed receiver data
90	GND	*GND*	Ground
91	CML	*RX4p*	High speed receiver data
92	CML	*RX4n*	High speed receiver data
93	GND	*GND*	Ground
94	CML	*RX5p*	High speed receiver data
95	CML	*RX5n*	High speed receiver data
96	GND	*GND*	Ground
97	CML	*RX6p*	High speed receiver data
98	CML	*RX6n*	High speed receiver data
99	GND	*GND*	Ground
100	CML	*RX7p*	High speed receiver data
101	CML	*RX7n*	High speed receiver data
102	GND	*GND*	Ground
103	CML	*RX8p*	High speed receiver data
104	CML	*RX8n*	High speed receiver data
105	GND	*GND*	Ground
106	CML	*RX9p*	High speed receiver data
107	CML	*RX9n*	High speed receiver data
108	GND	*GND*	Ground
109	-	*RX_DSCp*	Not Used
110	-	*RX_DSCn*	Not Used
111	GND	*GND*	Ground
112	GND	*GND*	Ground

113	CML	*TX0p*	High speed transmitter data
114	CML	*TX0n*	High speed transmitter data
115	GND	*GND*	Ground
116	CML	*TX1p*	High speed transmitter data
117	CML	*TX1n*	High speed transmitter data
118	GND	*GND*	Ground
119	CML	*TX2p*	High speed transmitter data
120	CML	*TX2n*	High speed transmitter data
121	GND	*GND*	Ground
122	CML	*TX3p*	High speed transmitter data
123	CML	*TX3n*	High speed transmitter data
124	GND	*GND*	Ground
125	CML	*TX4p*	High speed transmitter data
126	CML	*TX4n*	High speed transmitter data
127	GND	*GND*	Ground
128	CML	*TX5p*	High speed transmitter data
129	CML	*TX5n*	High speed transmitter data
130	GND	*GND*	Ground
131	CML	*TX6p*	High speed transmitter data
132	CML	*TX6n*	High speed transmitter data
133	GND	*GND*	Ground
134	CML	*TX7p*	High speed transmitter data
135	CML	*TX7n*	High speed transmitter data
136	GND	*GND*	Ground
137	CML	*TX8p*	High speed transmitter data
138	CML	*TX8n*	High speed transmitter data
139	GND	*GND*	Ground
140	CML	*TX9p*	High speed transmitter data
141	CML	*TX9n*	High speed transmitter data
142	GND	*GND*	Ground
143	-	*TX_DSCp*	Not Used
144	-	*TX_DSCn*	Not Used
145	GND	*GND*	Ground
146	-	*REFCLKp*	Not Used
147	-	*REFCLKn*	Not Used
148	GND	*GND*	Ground

Application Notes

Electrical interface: All signal interfaces follow the CFP MSA specification. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC. Hardware control and status reporting pins are 3.3V LVCOMS compatible. The MDIO interface pins are 1.2V LVCOMS compatible and should be pulled up with a 4.7 - 10kΩ resistor on the host board.

TX Disable: When the TX Disable pin is at logic HIGH, the transmitter optical output is disabled. The laser is also disabled if this line is left floating, as it is pulled high inside the transceiver.

Receiver Loss of Signal (RX_LOS): The Loss of Signal circuit monitors the level of the incoming optical signal and generates logic HIGH when an insufficient photocurrent is produced. The RX_LOS is the logic OR of the LOS signals from all the input receiving channels in the CFP module.

MDIO Interface: Upon module initialization, the alarm, control and monitor functions are available through the MDIO interface. The interface consists of 8 wires including 2 wires of MDC and MDIO, as well as 5 port address wires, and the Global Alarm wire.

MDC is the MDIO clock line driven by the host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The MDIO port address pins PRTADR0:4 are used for the system to address all of the CFP ports contained within a host system PRTADR0 corresponds to the LSB in the port addressing scheme. The 5-wire port address lines are driven by host to set the module port address which should match the address specified in the MDIO frame. The Global Alarm pin (GLB_ALRMn) is an output pin to the host. It asserts low on any fault/alarm/warning/status conditions that has been chosen. It is driven by the logic OR of all unmasked fault/alarm/warning/status conditions latched in the latched registers.

The data transfer protocol and the details of the mandatory and vendor specific data structures are defined in the CFP MSA Management Interface Specification draft 1.4.

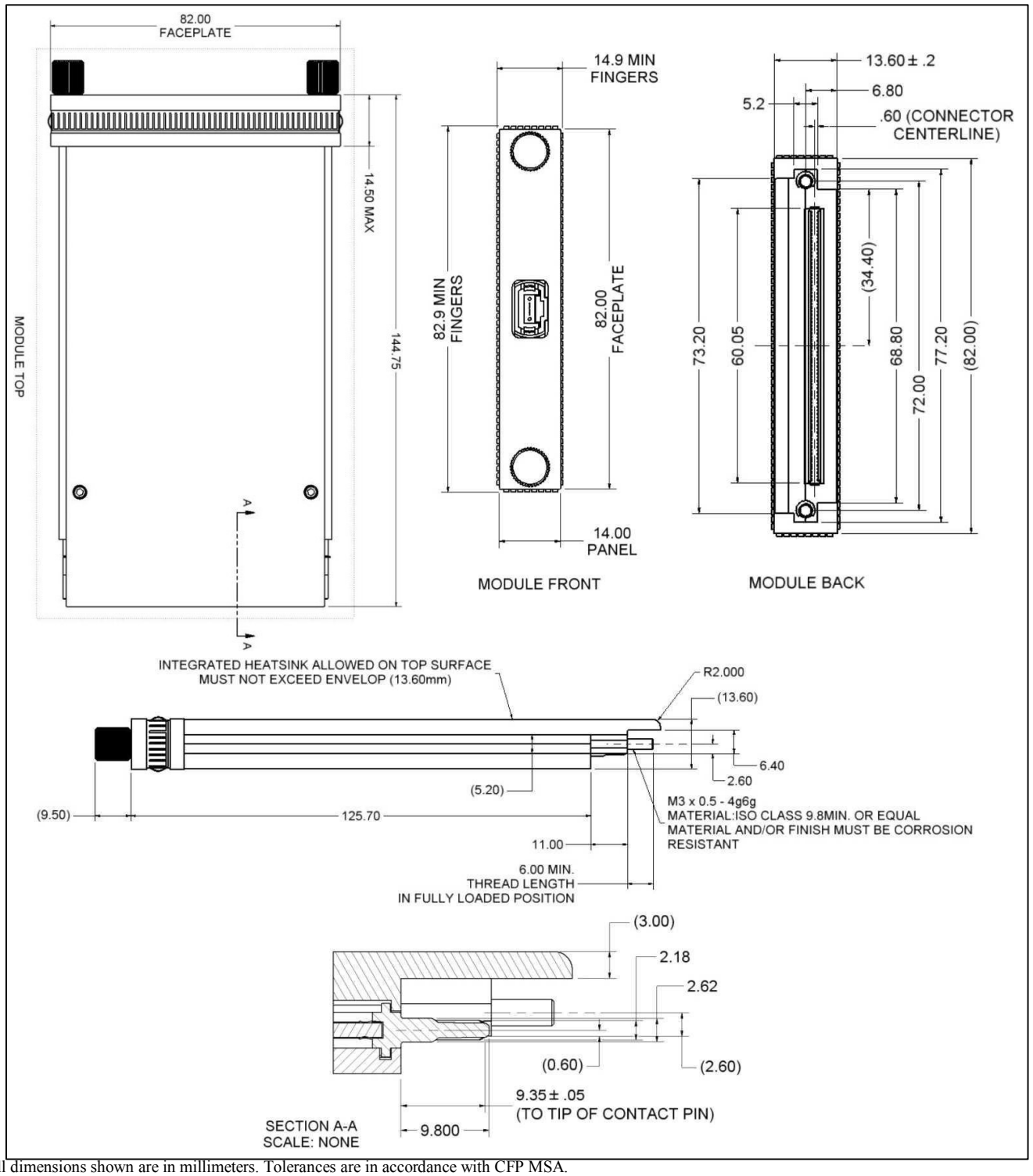
Power supply and grounding: The power supply line should be well-filtered. All power supply bypass capacitors should be as close to the transceiver module as possible.

Interfacing the Transceivers

Communication is via a set of non-MDIO hardware control and signal Pins and the MDIO interface. The MDIO management frame, set of CFP resisters and the set of rules for host control, module initialization, and signal exchange between Host and the transceiver is described in the document CFP MSA Management Interface Specification draft 1.4. Addresses from 0000h to 7FFFh are reserved for IEEE802.3. The CFP register space starts from 8000h to FFFFh.

CFP Register Allocation					
Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 Use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	86FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8FFF	RO	14x128	N/A	Reserved by CFP MSA.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control and DDM registers.
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA.
B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA.

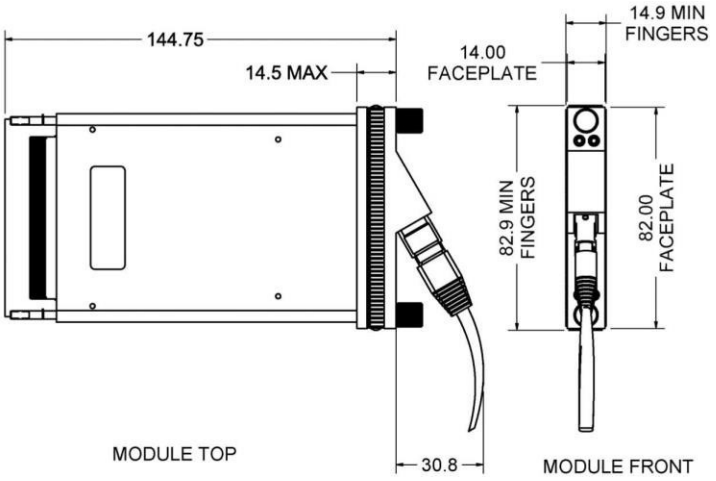
Module Outline



All dimensions shown are in millimeters. Tolerances are in accordance with CFP MSA.

Optional Angled MPO connector

An angled optical receptacle option is offered to minimize the distance the optical fiber cable extends from the faceplate to aid in meeting network equipment building system standards. Below is the mechanical drawing.



Ordering Information

Model Name	Operating Temperature	Nominal Wavelength (nm)	Distance (m)
HOLS-CFP85M1-M5D-CV	- 5°C to +70°C	850	100