

100Gb/s CFP Optical Transceiver Module Series

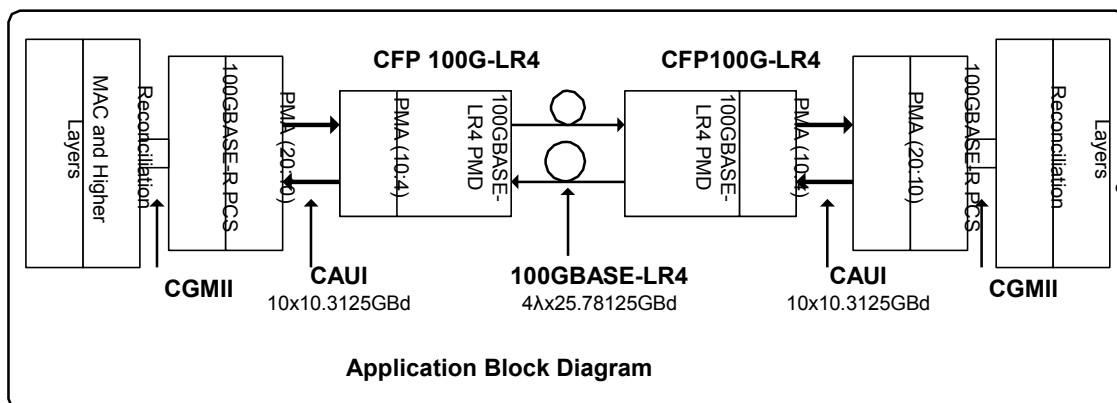
(100GBASE-LR4, ITU-T OTU-4, 1300nm 4-lane WDM, EA-DFB, PIN-PD)

Features

- 4-lane x 25.78Gb/s L-WDM Optical Interface
 - ◇ High quality and reliability optical sub-assemblies
 - ◇ 1300nm Cooled WDM EA-DFB Transmitter with optical MUX
 - ◇ High Sensitivity PIN-TIA with optical DEMUX
 - ◇ 1300nm band with 800GHz spacing LAN WDM grid up to 10km over a SMF
- IEEE802.3ba Compliant
 - ◇ IEEE802.3 Clause 88 100GBASE-LR4
 - ◇ CAUI(10x10G) Electrical Interface
 - ◇ MDIO Interface for module management
- OTU-4 Rate Operation
 - ◇ 4x27.95 Gb/s lane operation to support OTU-4
 - ◇ ITU-T 411-9D1F compatible 2km Optical I/F Option Available
- CFP MSA Compliant
 - ◇ Easy supply management for hot pluggability
 - ◇ CFP MSA Form Factor
 - ◇ 148pin Electrical Connector
 - ◇ Duplex SC or LC Receptacle
- Low Power Consumption
 - ◇ 3.3V single power supply, 16W max.

Applications

- 100GE Enterprise switches and routers
- Carrier Grade 100GE Core-routers
- Point to Point and Ring Application
- Inter Rack Connection
- Other high speed data connections



1 General Description

The series is the CFP optical transceiver module which is a hot pluggable form factor designed for high speed optical networking application. The series is designed for 100Gigabit Ethernet application and provides 100GBASE-LR4 compliant optical interface, CAUI electrical interface and MDIO module management interface. The series converts 10-lane 10.3Gb/s electrical data streams to 4-lane LAN-WDM 25.78Gb/s optical output signal and 4-lane LAN-WDM 25.78Gb/s optical input signal to 10-lane 10.3Gb/s electrical data streams. This 10-lane 10.3Gb/s electrical signal is fully compliant with 802.3ba CAUI specification and allows FR4 host PCB trace up to 25cm.

The high performance Cooled LAN-WDM EA-DFB transmitter and high sensitivity PIN receiver provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements..

2 Functional Description

The series CFP transceiver is a bi-directional module with a transmitter and receiver in one package. The series contains a duplex SC or LC connector for the optical interface and a 148-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of CFP transceiver. The series contains electrical 10:4 Mux, 4:10 DeMux, 4-lane optical transmitter, 4-lane optical receiver and module management block including MDIO interface.

Transmitter Operation

The transceiver module receives 10-lane 10.3Gb/s CAUI electrical inputs. CDR reshapes and retimes received electrical signal to compensate the degraded electrical signal which comes through host board and host connectors. A reference clock from host card is 1/64 frequency of TX CAUI lane rate and should be synchronized to TX CAUI input signal. 10 to 4 electrical Mux synthesizes 4-lane rate clock from the reference clock and multiplexes

10-lane received signals to 4-lane electrical signals. The multiplexed 4-lane signals are fed to the transmitters. The four transmitters convert 4-lane signals to an optical signal through 4 Laser drivers and Lasers diodes which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each Laser launches optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into one fiber by 4 to1 Optical WDM MUX. The optical output power is held constant by an automatic power control (APC) circuit. The transmitters output can be turned off by TX_DIS hardware signal and/or through MDIO module management Interface.

Receiver Operation

The series receives 4-lane LANWDM optical signals. The optical signals are de-multiplexed by 1 to 4 optical DEMUX and fed into each Receiver Optical Sub-Assembly. Each ROSA converts optical signal to electrical signal. The regenerated electrical signals are retimed and de-jittered by the CDRs inside the 4:10 electrical DeMux. The retimed 4-lane received signals are de-multiplex to 10-lane signals by the 4 to 10 electrical DeMux. The 10-lane signals are compliant with IEEE CAUI interface requirements. Each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be launched.

Management Data I/O (MDIO)

The series supports the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PORT_ADDR0-4) into the module.

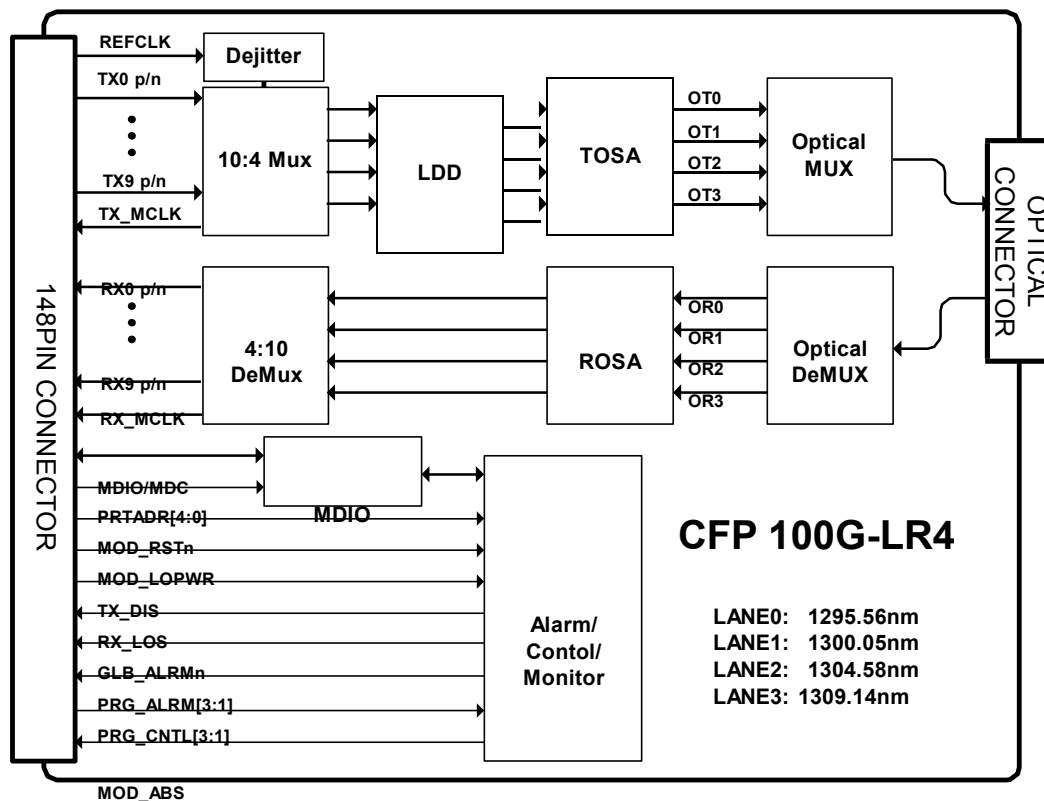
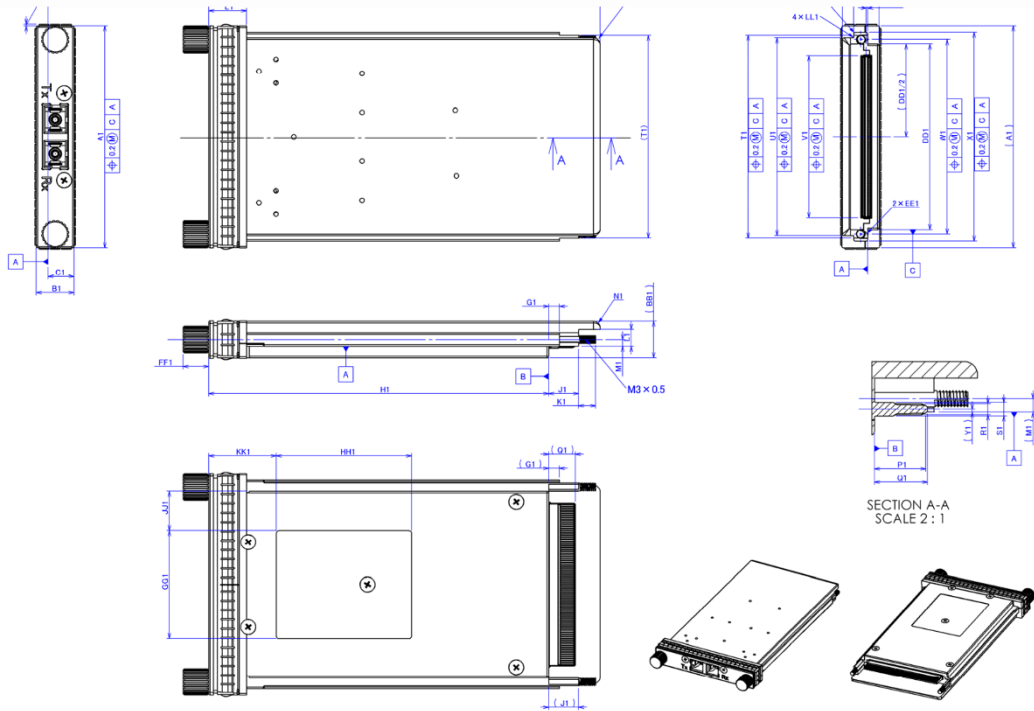


Figure 2.1. Functional Block Diagram

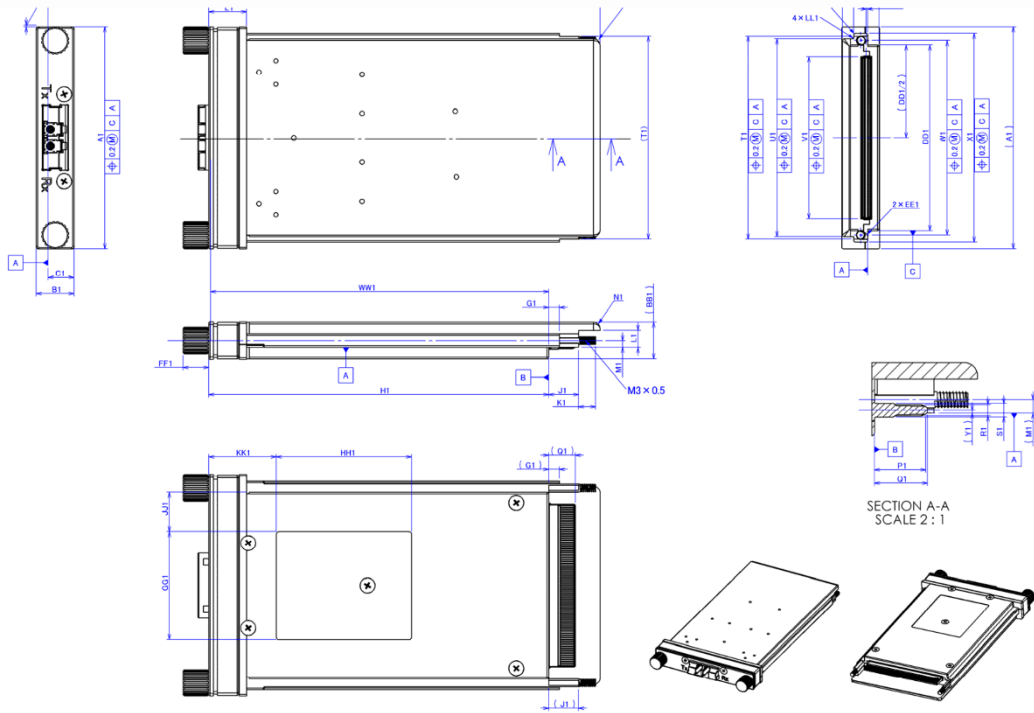
3 Package Dimensions

Figure 3.1 shows the package dimensions of CFP. The CFP transceiver is designed to be compliant with CFP MSA specification.



Dimensions in mm

Figure 3.1. (a) SC with Flat Top Package Drawing



Dimensions in mm

Figure 3.1. (b) LC with Flat Top Package Drawing

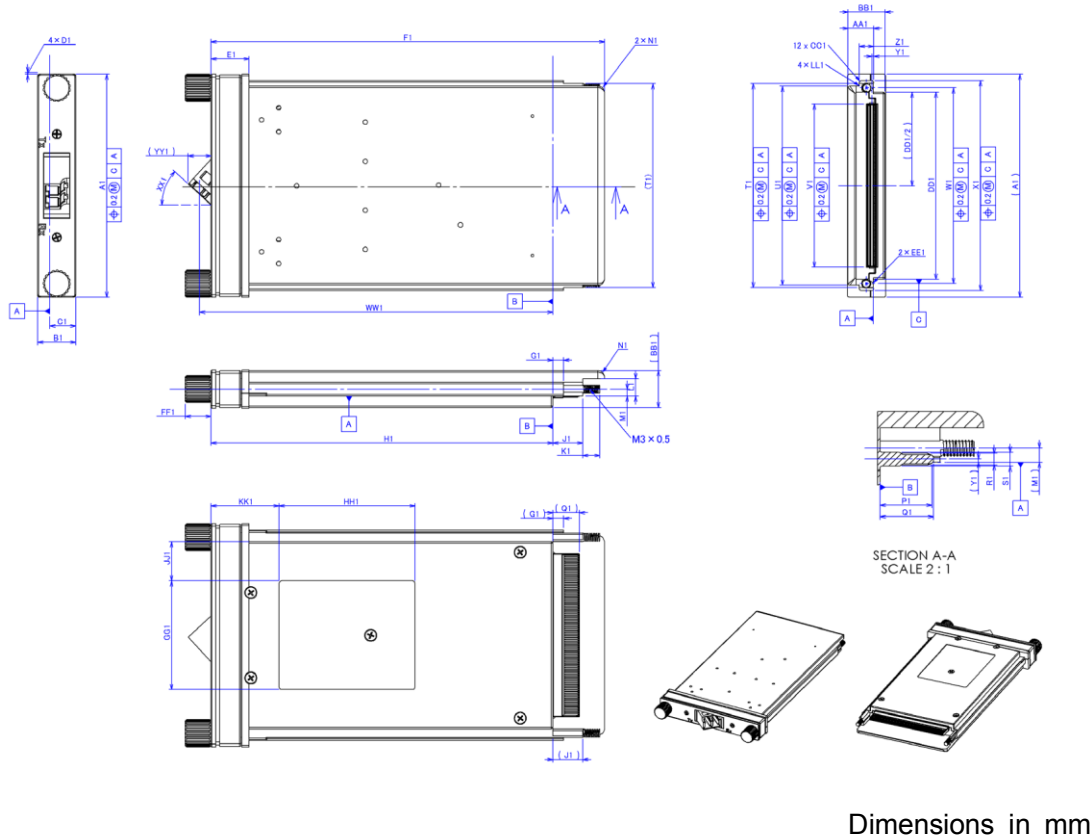


Figure 3.1. (c) LC Angled with Flat Top Package Drawing

Table 3.1. Package dimensions

MODULE DIMENSIONS				Note
KEY	VALUE	TOLERANCE	DESCRIPTION	
A1	82.00	±0.10	WIDTH OF MODULE FACEPLATE, OVERALL	
B1	14.00	±0.10	HEIGHT OF MODULE FACEPLATE, OVERALL	
C1	9.60	±0.20	HEIGHT OF MODULE FACEPLATE TO DATUM -A-	
D1	0.65	MIN.	HEIGHT OF EMI SPRING FINGERS	
E1	14.50	MAX.	LENGTH OF MODULE FACEPLATE, OVERALL	
F1	144.75	±0.20	LENGTH OF MODULE, OVERALL	
G1	4.80	MAX.	LENGTH OF MODULE RAIL SHOULDER	
H1	125.70	±0.20	DISTANCE FROM MODULE FACEPLATE TO HARDSTOP DATUM -B-	
J1	11.00	±0.20	DISTANCE FROM CONNECTOR PROTECTOR TO HARDSTOP DATUM -B-	
K1	6.00	±0.50	M3 THUMBSCREW THREAD LENGTH IN FULLY LOADED POSITION	
L1	6.40	±0.20	DISTANCE FROM DATUM -A- TO BOTTOM SURFACE OF MODULE TAIL	
M1	2.60	±0.20	DISTANCE FROM DATUM -A- TO CENTERLINE OF M3 THUMBSCREW HOLE	
N1	R2.00	MIN.	TOP MODULE LEAD-IN RADIUS	
P1	9.08	±0.15	LENGTH OF CONNECTOR CONTACT PIN FROM DATUM -B-	
Q1	9.80	±0.08	LENGTH OF CONNECTOR END FROM DATUM -B-	
R1	2.18	±0.08	CONNECTOR TIP THICKNESS, OVERALL	
S1	2.62	±0.08	CONNECTOR SHOULDER THICKNESS, OVERALL	
T1	75.00	±0.20	WIDTH OF MODULE CONNECTOR PROTECTOR, OVERALL	
U1	73.20	±0.20	WIDTH, TOP SHOULDER, MODULE, OVERALL	
V1	60.05	±0.08	WIDTH, CONNECTOR, OVERALL	
W1	72.00	±0.20	CENTERLINE TO CENTERLINE DISTANCE OF M3 THUMB SCREW HOLES	
X1	77.20	±0.20	WIDTH, MODULE BODY, OVERALL	
Y1	0.60	±0.15	DATUM -A- TO CENTERLINE OF CONNECTOR	
Z1	5.20	±0.20	HEIGHT, RAIL SHOULDER, MODULE, OVERALL	
AA1	9.40	±0.20	DATUM -A- TO TOP OF MODULE	
BB1	13.60	±0.20	HEIGHT, MODULE BODY, OVERALL	
CC1	R0.6	±0.10	MODULE OUTSIDE CORNER RADIUS	
DD1	68.80	±0.20	WIDTH, MODULE BOTTOM, OVERALL	
EE1	R2.60	±0.20	RADIUS, CLEARANCE, MODULE, CONNECTOR PROTECTOR FEATURE	
FF1	9.50	±0.50	THUMBSCREW HEIGHT FROM MODULE FACEPLATE TOP FRONT SURFACE	
GG1	40.00	±0.20	LABEL RECESS WIDTH	
HH1	50.00	±0.20	LABEL RECESS LENGTH	
JJ1	14.40	±0.20	LABEL RECESS TO SIDE OF MODULE	
KK1	25.00	±0.20	LABEL RECESS TO MODULE FACEPLATE	
LL1	R0.4	MAX.	MODULE INSIDE CORNER RADIUS	
WW1	125.00	±0.50	CFP module stopper to LC connector Latch	1
WW1	129.90	±0.50	CFP module locking mechanism to the LC connector Latch	2
XX1	45°	±5°	Angular difference between module center and LC receptacle	2
YY1	8.50	Reference	Distance from module faceplate to LC receptacle	2

1: Apply to LC Duplex Option

2: Apply to LC Angled Duplex Option

Table 3.2. CFP Mechanical Characteristics

	Max.	Unit	Notes
Weight	350	g	
Flatness	0.15	nm	
Roughness	6.3	Ra	

4 Pin Assignment and Pin Description

4.1. CFP Transceiver Electrical Pin Assignment

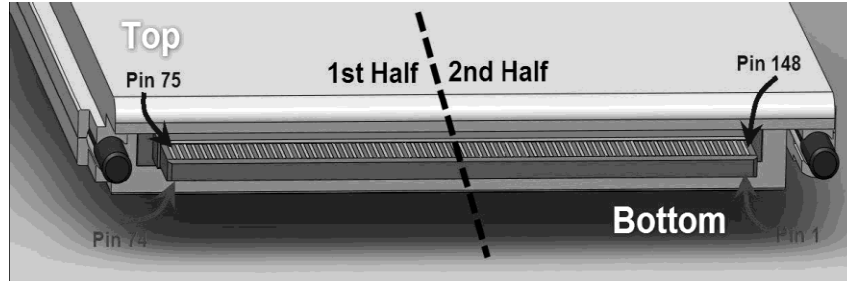


Figure 4.1. CFP Transceiver Electrical Pin Numbering

Table 4.1. CFP Transceiver Electrical Pin Assignment

Top Row		Bottom Row		Top Row		Bottom Row	
2nd Half		2nd Half		1st Half		1st Half	
PIN#	Name	PIN#	Name	PIN#	Name	PIN#	Name
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	NC	39	MOD_RST n
146	REFCLKp	3	3.3V_GND	109	NC	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	NC	5	3.3V_GND	107	RX9n	42	PRTADR4
143	NC	6	3.3V	106	RX9p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	TX9n	8	3.3V	104	RX8n	45	PRTADR1
140	TX9p	9	3.3V	103	RX8p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	TX8n	11	3.3V	101	RX7n	48	MDC
137	TX8p	12	3.3V	100	RX7p	49	GND
136	GND	13	3.3V	99	GND	50	NUC (note1)
135	TX7n	14	3.3V	98	RX6n	51	NUC (note1)
134	TX7p	15	3.3V	97	RX6p	52	GND
133	GND	16	3.3V_GND	96	GND	53	NUC (note1)
132	TX6n	17	3.3V_GND	95	RX5n	54	NUC (note1)
131	TX6p	18	3.3V_GND	94	RX5p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	TX5n	20	3.3V_GND	92	RX4n	57	3.3V_GND
128	TX5p	21	NUC (note1)	91	RX4p	58	3.3V_GND
127	GND	22	NUC (note1)	90	GND	59	3.3V_GND
126	TX4n	23	GND	89	RX3n	60	3.3V
125	TX4p	24	TX_M CLKn (note2)	88	RX3p	61	3.3V
124	GND	25	TX_M CLKp (note2)	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	NUC (note1)	85	RX2p	64	3.3V
121	GND	28	NUC (note1)	84	GND	65	3.3V
120	TX2n	29	NUC (note1)	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALARM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALARM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALARM3	77	RX_M CLKn (note2)	72	3.3V_GND
113	TX0p	36	TX_DIS	76	RX_M CLKp (note2)	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

1: These pins are internally used and NOT allowed to connect any signal and power supply or GND.

2: These output signals are disabled unless MCLK output is enabled via MDIO.

4.2 Host PCB CFP Foot Print

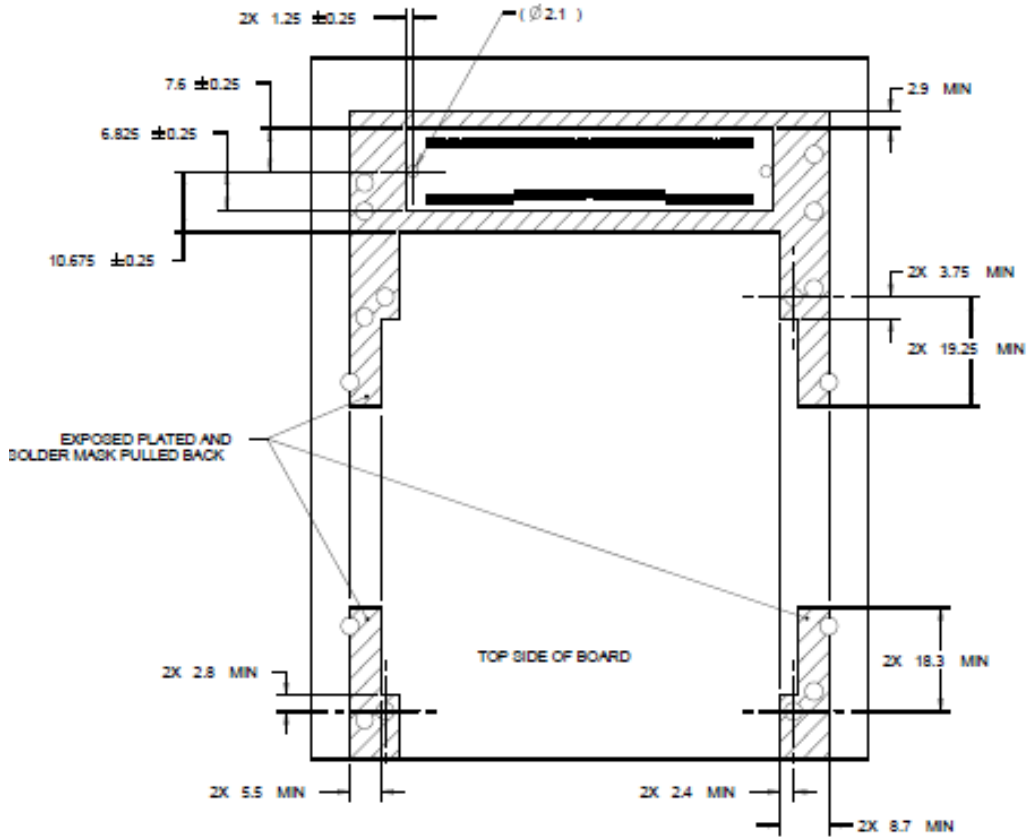


Figure 4.2. Host PCB CFP Foot Print

Table 4.2. Host Connector Assembly Information

Part Name	Part Number	Supplier
External Bracket Assembly	2057626-1	Tyco Electronics
Guide Rail	2057592-2	Tyco Electronics
Host Connector Cover	2057631-1	Tyco Electronics
Backer Plate Assembly	2057930-1	Tyco Electronics
Host Connector	2057630-1	Tyco Electronics

4.3 Pin Descriptions

Table 4.3. Pin Description

PIN#	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			3.3V Module Supply Voltage
8	3.3V			3.3V Module Supply Voltage
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V			3.3V Module Supply Voltage
14	3.3V			3.3V Module Supply Voltage
15	3.3V			3.3V Module Supply Voltage
16	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	NUC			Module Vendor I/O. Must No Connect at host board
22	NUC			Module Vendor I/O. Must No Connect at host board
23	GND			
24	TX_MCLKn	O		TX Monitor Clock Output (Negative)
25	TX_MCLKp	O		TX Monitor Clock Output (Positive)
26	GND			
27	NUC			Module Vendor I/O. Must No Connect at host board
28	NUC			Module Vendor I/O. Must No Connect at host board
29	NUC			Module Vendor I/O. Must No Connect at host board
30	PRG_CNTL1	I	LVC MOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LVC MOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
32	PRG_CNTL3	I	LVC MOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
33	PRG_ALARM1	O	LVC MOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
34	PRG_ALARM2	O	LVC MOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
35	PRG_ALARM3	O	LVC MOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LVC MOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RST _n	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVC MOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRM _n	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	NUC			Module Vendor I/O. Must No Connect at host board
51	NUC			Module Vendor I/O. Must No Connect at host board
52	GND			
53	NUC			Module Vendor I/O. Must No Connect at host board
54	NUC			Module Vendor I/O. Must No Connect at host board
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			3.3V Module Supply Voltage
62	3.3V			3.3V Module Supply Voltage
63	3.3V			3.3V Module Supply Voltage
64	3.3V			3.3V Module Supply Voltage
65	3.3V			3.3V Module Supply Voltage
66	3.3V			3.3V Module Supply Voltage
67	3.3V			3.3V Module Supply Voltage
68	3.3V			3.3V Module Supply Voltage
69	3.3V			3.3V Module Supply Voltage
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
75	GND			
76	RX_MCLKp	O		RX Monitor Clock Output (Positive)
77	RX_MCLKn	O		RX Monitor Clock Output (Negative)
78	GND			
79	RX0p	O	HS I/O	Lane 0 Receiver Output (Positive)
80	RX0n	O	HS I/O	Lane 0 Receiver Output (Negative)
81	GND			
82	RX1p	O	HS I/O	Lane 1 Receiver Output (Positive)
83	RX1n	O	HS I/O	Lane 1 Receiver Output (Negative)
84	GND			
85	RX2p	O	HS I/O	Lane 2 Receiver Output (Positive)
86	RX2n	O	HS I/O	Lane 2 Receiver Output (Negative)
87	GND			
88	RX3p	O	HS I/O	Lane 3 Receiver Output (Positive)
89	RX3n	O	HS I/O	Lane 3 Receiver Output (Negative)
90	GND			
91	RX4p	O	HS I/O	Lane 4 Receiver Output (Positive)
92	RX4n	O	HS I/O	Lane 4 Receiver Output (Negative)
93	GND			
94	RX5p	O	HS I/O	Lane 5 Receiver Output (Positive)
95	RX5n	O	HS I/O	Lane 5 Receiver Output (Negative)
96	GND			
97	RX6p	O	HS I/O	Lane 6 Receiver Output (Positive)
98	RX6n	O	HS I/O	Lane 6 Receiver Output (Negative)
99	GND			
100	RX7p	O	HS I/O	Lane 7 Receiver Output (Positive)
101	RX7n	O	HS I/O	Lane 7 Receiver Output (Negative)
102	GND			
103	RX8p	O	HS I/O	Lane 8 Receiver Output (Positive)
104	RX8n	O	HS I/O	Lane 8 Receiver Output (Negative)
105	GND			
106	RX9p	O	HS I/O	Lane 9 Receiver Output (Positive)
107	RX9n	O	HS I/O	Lane 9 Receiver Output (Negative)
108	GND			
109	NC			Not Connected Internally
110	NC			Not Connected Internally
111	GND			

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
112	GND			
113	TX0p	I	HS I/O	Lane 0 Transmitter Input (Positive)
114	TX0n	I	HS I/O	Lane 0 Transmitter Input (Negative)
115	GND			
116	TX1p	I	HS I/O	Lane 1 Transmitter Input (Positive)
117	TX1n	I	HS I/O	Lane 1 Transmitter Input (Negative)
118	GND			
119	TX2p	I	HS I/O	Lane 2 Transmitter Input (Positive)
120	TX2n	I	HS I/O	Lane 2 Transmitter Input (Negative)
121	GND			
122	TX3p	I	HS I/O	Lane 3 Transmitter Input (Positive)
123	TX3n	I	HS I/O	Lane 3 Transmitter Input (Negative)
124	GND			
125	TX4p	I	HS I/O	Lane 4 Transmitter Input (Positive)
126	TX4n	I	HS I/O	Lane 4 Transmitter Input (Negative)
127	GND			
128	TX5p	I	HS I/O	Lane 5 Transmitter Input (Positive)
129	TX5n	I	HS I/O	Lane 5 Transmitter Input (Negative)
130	GND			
131	TX6p	I	HS I/O	Lane 6 Transmitter Input (Positive)
132	TX6n	I	HS I/O	Lane 6 Transmitter Input (Negative)
133	GND			
134	TX7p	I	HS I/O	Lane 7 Transmitter Input (Positive)
135	TX7n	I	HS I/O	Lane 7 Transmitter Input (Negative)
136	GND			
137	TX8p	I	HS I/O	Lane 8 Transmitter Input (Positive)
138	TX8n	I	HS I/O	Lane 8 Transmitter Input (Negative)
139	GND			
140	TX9p	I	HS I/O	Lane 9 Transmitter Input (Positive)
141	TX9n	I	HS I/O	Lane 9 Transmitter Input (Negative)
142	GND			
143	NC			Not Connected Internally
144	NC			Not Connected Internally
145	GND			
146	REFCLKp	I		Reference Clock Input (Positive)
147	REFCLKn	I		Reference Clock Input (Negative)
148	GND			

5 Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH		85	%	
Supply Voltage	Vcc	-0.3	3.6	V	
Voltage on any 3.3V LVCMOS pin	V _{LVCMOS}	-0.3	V _{cc} +0.3	V	
Voltage on any 1.2V LVCMOS pin	V _{LVCMOS}	-0.3	1.65	V	
Receiver Input Optical Power each lane	Mip		5.5	dBm	

Table 5.2. Recommended Operating Conditions and supply requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	-5	70	degC	
Relative Humidity (non-condensing)	Rhop		85	%	
Power Supply Voltage	Vcc	3.135	3.465	V	
Power Supply Current for 3.3V			5.1	A	
Total Power Dissipation	Pw	-	16	W	
Low Power Mode dissipation	Plow	-	2	W	
In-rush Current (Class 1 and 2)	I-inrush	-	50	mA/us	
Turn-off rush Current (Class 1 and 2)	I-turnoff	-50	-	mA/us	
Power Supply Noise	Vrip	-	2	%	DC-1MHz
		-	3	%	1-10MHz

6 Electrical Interface

6.1 Electrical High Speed I/O Interface

Table 6.1.1. CAUI Input Interface

CAUI Receiver Parameters	symbol	Min	Typ	Max	Units	Note
Signal Rate Per Lane			10.3125		Gb/s	
Signal Rate tolerance		-100		100	ppm	
AC Common Mode Voltage Tolerance, RMS	CMVLTac			20	mV	
Minimum Differential Input Return Loss	Rldiff	IEEE802.3ba Equation 83B-5			dB	
Total Input Jitter Tolerance	Tjin			0.62	UI	
Deterministic Input Jitter Tolerance	Tdin			0.42	UI	
Transmitter Input Eye Mask (X1, X2)		(0.31, 0.5)			UI	1
Transmitter Input Eye Mask (Y1, Y2)		(42.5, 425)			mV	1

Table 6.1.2 CAUI Output Interface

CAUI Driver Parameters	symbol	Min	Typ	Max	Units	Note
Signal Rate Per Lane			10.3125		Gb/s	
Signal Rate tolerance		-100		100	ppm	
Single-end Output Voltage	Vosingle	-0.4		4	V	
Output AC Common Mode Voltage, RMS	Vocomac			15	mV	
Output Rise and Fall Time (20%-80%)	Trfl	24			ps	
Minimum Differential Output Return Loss	Rldiff	IEEE802.3ba Equation 83B-6			dB	
Total Output Jitter	Tjo			0.4	UI	
Deterministic Output Jitter	Tdo			0.25	UI	
Receiver Output Eye Mask (X1, X2)		(0.2, 0.5)			UI	2
Receiver Output Eye Mask (Y1, Y2)		(136, 380)			mV	2

1: Refer to Figure 6.1.1, 2: Refer to Fig.6.1.2

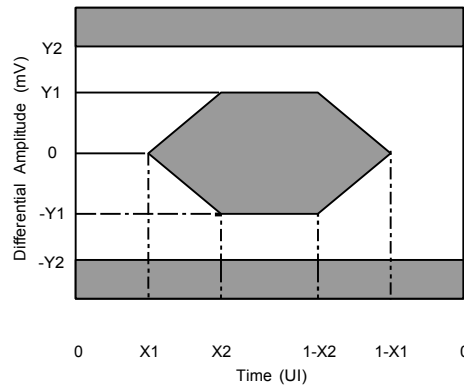
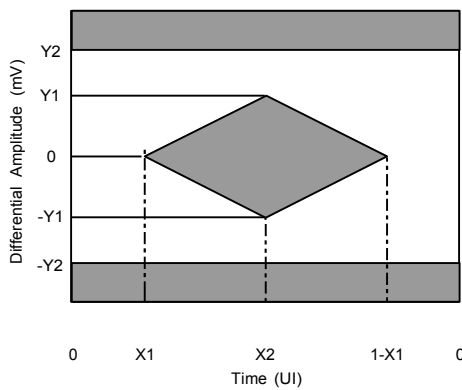


Figure 6.1.1. CAUI Receiver Eye Mask Figure 6.1.2. CAUI Transmitter Eye Mask

Table 6.1.3 Reference Clock Interface

The SCF1001L4 requires stable Reference clocks before de-asserting MOD_LOPWR.

Parameter	symbol	Min	Typ	Max	Units	Note
Impedance	Zd	80	100	120	ohm	
Frequency		1/64 of host lane rate				
Frequency Stability	Xf	-100		100	ppm	1
		-20.0		20		2
Input Differential Voltage	VDIFF	400		1200	mV	3
RMS Jitter	σ			10	ps	4
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10/90%	tr/f	200		1250	ps	5

1: For Ethernet applications, 2: For Telecom applications, 3: Peak to Peak Differential

4: Random Jitter. Over frequency band of 10kHz < f < 10MHz, 5: 1/64 of electrical lane

Table 6.1.4 Transmitter and Receiver Monitor Clock Interface

Parameter	symbol	Min	Typ	Max	Units	Note
Impedance	Zd	80	100	120	Ω	
Frequency		1/8 of network lane rate				
Output Differential Voltage	VDIFF	400		1200	mV	1
Clock Duty Cycle		40.0		60	%	

1: Peak to Peak Differential

6.2 Electrical Low Speed I/O interface

Table 6.2.1. 3.3V CMOS DC parameters

(MOD_RSTn, MOD_LOPWR, TX_DIS, PRG_CNTL, MOD_ABS, RX_LOS, GLB_ALRMn, PRG_ALARM)

Parameter	symbol	Min	Typ	Max	Units	Note
Input High Voltage	Vih	2		Vcc+0.3	V	
Input Low Voltage	Vil	-0.3		0.8	V	
Input Leakage Current	IIN	-10		10	μA	
Output High Voltage (IOH=-100uA)	Voh	Vcc-0.2		Vcc+0.3	V	
Output Low Voltage (IOL=100uA)	Vol	-0.3		0.2	V	
Minimum Pulse Width of Control Pin Signal	t_CNTL	100			μS	

Table 6.2.2. 1.2V CMOS DC parameters (MDIO, MDC, PRTADR4:0)

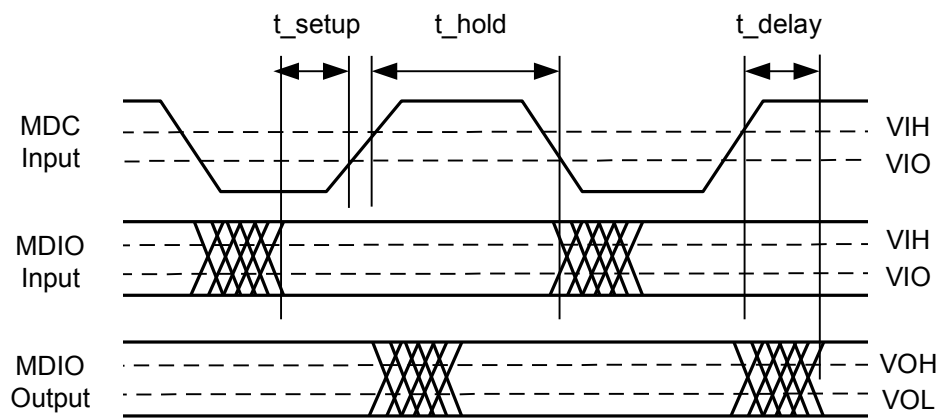
Parameter	symbol	Min	Typ	Max	Units	Note
Input High Voltage	Vih	0.84		1.5	V	
Input Low Voltage	Vil	-0.3		0.36	V	
Input Leakage Current	IIN	-100		100	μA	
Output High Voltage	Voh	1.0		1.5	V	
Output Low Voltage	Vol	-0.3		0.2	V	
Output high current (Vi = 1.0V)	Iioh			-4	mA	
Output low current (Vi = 0.2V)	Iiol	4			mA	
Input Capacitance	CI			10	pF	

Table 6.2.3. Timing Parameters for CFP Hardware Signal Pins

Parameter	Symbol	Min	Max	Units	Note
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert		10	s	
Receiver Loss of Signal Assert Time	t_loss_assert		100	μs	
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	μs	
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	
Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert		150	ms	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled (TX_DIS asserted)	t_deassert		100	μs	
Transmitter Enabled (TX_DIS de-asserted)	t_assert		2	ms	

Table 6.2.4. MDIO and MDC AC parameters

Parameter	symbol	Min	Typ	Max	Units	Note
MDC clock Frequency	fMDC	0.1		4	MHz	
MDC clock period	tprd	250		10000	ns	
MDIO data hold time	Thold	10			ns	
MDIO data setup time	Tsetup	10			ns	
MDC high and low time	twidth	40		60	%	
		160			ns	
Delay from MDC rising edge to MDIO data change	Tdelay			175	ns	
MDIO/MDC termination in CFP	Zt	100			kOhm	



.2.1. MDIO and MDC AC parameters

Table 7.1. (a) Optical Interface 100GBASE-LR4

<i>CFP 100GBASE-LR4</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Fiber type			SMF			
Signaling speed, each Client/Line		10.3125/ 25.78125± 100ppm			Gbps	
Operating Reach 1			2 – 10k		m	
Lane wavelength (range): L0	L0	1294.53	1295.56	1296.59	nm	
Lane wavelength (range): L1	L1	1299.02	1300.05	1301.09	nm	
Lane wavelength (range): L2	L2	1303.54	1304.58	1305.63	nm	
Lane wavelength (range): L3	L3	1308.09	1309.14	1310.19	nm	
<i>Transmitter Optical Interface</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
SMSR	SMSR	30		-	dB	
Total average launch power (max)	Pot	10.5			dBm	
Average launch power, each lane (max)	Pavemax	4.5			dBm	
OMA, each lane (max)	Pmoamax	4.5			dBm	
OMA, each lane (min)	Pomamin	-1.3			dBm	
OMA Difference between any two lanes	TdOMA			5.0	dB	
OMA - TDP, each lane	OMAtdp	-2.3			dBm	
Transmitter and Dispersion Penalty (TDP), each lane (max)	TDP	2.2			dB	
Average power Disabled, each lane (max)	Podis	-30			dBm	
Extinction Ratio	ER1	4	5.5	-	dB	
RIN12OMA	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	Torlt			20	dB	
Transmitter Refractance (max)	Toref	-12			dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	PM	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1
<i>Receiver Optical Interface</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Damage threshold	Pindm	5.5			dBm	
Average receive power, each lane (max)	Piavemax	4.5			dBm	
Receive power, each lane (OMA) (max)	Pomamax	4.5			dBm	
OMA Difference between any two lanes	RdOMA			5.5	dB	
Receiver reflectance (max)	Roref	-26			dB	
Receiver sensitivity (OMA), each lane (max)	Pomamin	-8.6			dBm	
Stressed sensitivity in OMA Vertical eye closure penalty 1.8dB Stressed eye jitter 0.3 UI	OMAst			-6.8	dBm	
Rx-Lane LOS Assert	LOSas		-18		dBm	
Rx-Lane LOS Deassert	LOSdea		-15		dBm	
Rx-Lane LOS Hysteresis	Sdhys	0.5			dB	

1: Refer to Fig.7.1

b) Optical Interface 100GBASE-LR4 and OTU-4 Multi-rate

<i>CFP 100GBASE-LR4 & OTU-4 Multi-Rate</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Fiber type			SMF			
Signaling speed, each Client/Line		10.3125/25.78125± 100ppm			Gbps	
Signaling speed, each Client/Line		11.1809/27.9525 ± 20ppm			Gbps	
Operating Reach 1			2 – 10k		m	1, 2
Operating Reach 2			– 7k		m	3
Lane wavelength (range): L0	L0	1294.53	1295.56	1296.59	nm	
Lane wavelength (range): L1	L1	1299.02	1300.05	1301.09	nm	
Lane wavelength (range): L2	L2	1303.54	1304.58	1305.63	nm	
Lane wavelength (range): L3	L3	1308.09	1309.14	1310.19	nm	
<i>Transmitter Optical Interface</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
SMSR	SMSR	30		-	dB	
Total average launch power (max)	Pot	8.9			dBm	
Average launch power, each lane (max)	Poln	2.9			dBm	
Average launch power, each lane (min)	Poln	-2.5			dBm	
OMA, each lane (max)	OMA	4.5			dBm	
OMA, each lane (min)	OMA	-1.2			dBm	
OMA Difference between any two lanes	TdOMA			5.0	dB	
OMA - TDP, each lane	OMAtdp	-2.3			dBm	4
Transmitter and Dispersion Penalty (TDP), each lane (max)	TDP	2.2			dB	4
Average power Disabled, each lane (max)	Podis	-30			dBm	
Extinction Ratio	ER1	7			dB	
RIN _{12OMA}	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	Torlt			20	dB	
Transmitter Reflectance (max)	Toref	-12			dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	PM	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				5
<i>Receiver Optical Interface</i>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Damage threshold	Pindm	5.5			dBm	
Average receive power, each lane (max)	Pavemax	4.5			dBm	
Receive power, each lane (OMA) (max)	Pomamax	4.5			dBm	
OMA Difference between any two lanes	RdOMA			5.5	dB	
Receiver reflectance (max)	Roref			-26	dB	
Receiver Sensitivity Average Power, each lane	Prmin	-10.3			dBm	6
Receiver Sensitivity (OMA) , each lane	Pomamin	-9.1			dBm	6
Stressed sensitivity in OMA	OMAst	-6.8			dBm	4
Vertical eye closure penalty 1.8dB						
Stressed eye jitter 0.3 UI						
Rx-Lane LOS Assert	LOSas		-18		dBm	
Rx-Lane LOS Deassert	LOSdea		-15		dBm	
Rx-Lane LOS Hysteresis	Sdhys	0.5			dB	

1: 100GBASE-LR4, 2: OTU-4 with FEC, 3: OTU-4 without FEC, 4: Only for 100GBASE-LR4,

5: Refer to Fig.7.1, 6: OTU-4 Rate without FEC, BER < 10⁻¹², ER > 7dB

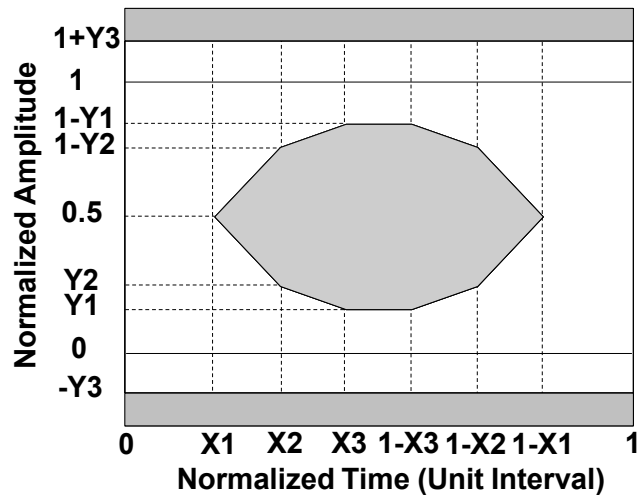
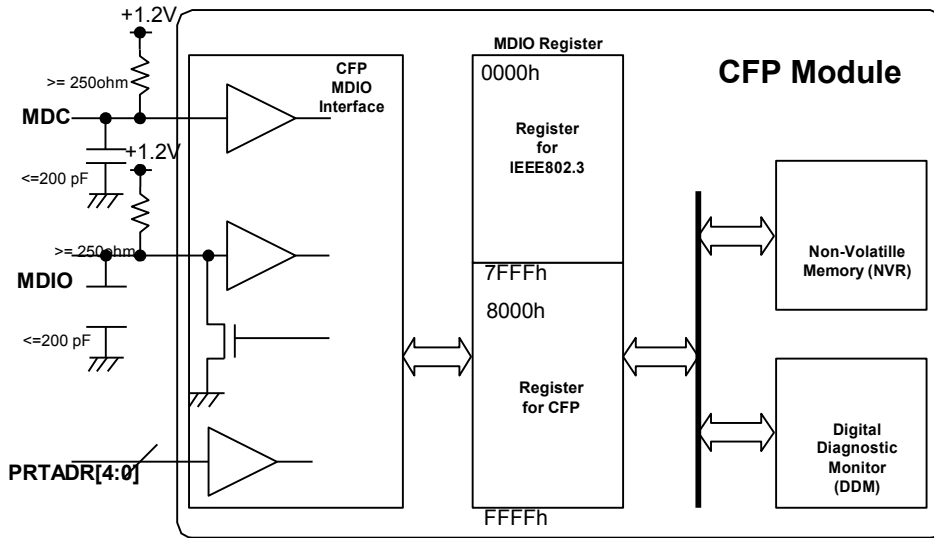


Fig 7.1. Transmission eye mask definition

8 MDIO and Non-Volatile Registers Map

8.1 MDIO Interface and CFP Register Allocation



Capacitor represents stray capacity 600ohm pull-up is preferred

Figure 8.1. CFP MDIO Interface

Table 8.1. CFP Register Allocation

Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 Use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	86FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8FFF	RO	14x128	N/A	Reserved by CFP MSA.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control / DDM registers.
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA.
B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA.

8.2 Non-Volatile Register (NVR) Map

Table 8.2.1. CFP NVR-1 (Example: SCF1011L4LNGG01)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
8000	1	RO		Module Identifier		0Eh	0E: CFP	N/A
8001	1	RO		Extended Identifier		54h	01010100	N/A
			7	Power Class	0	01b: Class 2 (<=16W)	N/A	
			6		1	N/A		
			5	Lane Ratio Type	0	01b: n : m Gearbox Type	N/A	
			4		1		N/A	
			3		0		N/A	
			2	WDM Type	1	010b: LAN-WDM	N/A	
			1		0		N/A	
			0	CLEI Presence	0	0: No CLEI code present	N/A	
8002			1	RO		Connector Type Code		07h
8003	1	RO		Ethernet Application Code		01h	01: 100GBASE-LR4	N/A
8004	1	RO		Fiber Channel Application Code		00h	00h: Undefined type	N/A
8005	1	RO		Copper Link Application Code		00h	00h: Undefined type	N/A
8006	1	RO		SONET/SDH Application Code		00h	00: Undefined type	N/A
8007	1	RO		OTN Application Code		08h	08h: 411-9D1F (OLT4.4) 00h: Not supported	N/A
8008	1	RO		Additional Capable Rates Supported		18h	00011000	N/A
			7	Reserved	0	0: Reserved	N/A	
			6	Reserved	0	0: Reserved	N/A	
			5	Reserved	0	0: Reserved	N/A	
			4	111.8 Gbps	1	1: Supported 0: Not supported	N/A	
			3	103.125 Gbps	1	1: Supported	N/A	
			2	41.25 Gbps	0	0: Not supported	N/A	
			1	43 Gbps	0	0: Not supported	N/A	
0	39.8 Gbps	0	0: Not supported	N/A				
8009	1	RO		Number of Lanes Supported		4Ah	01001010	N/A
			7	Number of Network Lanes	0	0100: 4 lanes	N/A	
			6		1			
			5		0			
			4	Number of Host Lanes	0	1010: 10 lanes	N/A	
			3		1			
			2		0			
			1		1			
0	0							
800A	1	RO		Media Properties		11h	00010001	N/A
			7	Media Type	0	00b: SMF	N/A	
			6	Directionality	0	0: Normal	N/A	
			5	Optical Mux and DeMux	1	1: with optical MUX/DEMUX	N/A	
			4	Active Fiber per Connector	0	0001b: 1 TX lane and 1 RX lane	N/A	
			3		0			
			2		0			
1	0							
0	1							
800B	1	RO		Maximum Network Lane Bit Rate		8Ch	8Ch: 27.9529Gbps / 0.2 81h: 25.78125Gbps / 0.2	0.2 Gbps
800C	1	RO		Maximum Host Lane Bit Rate		38h	38h: 11.1809Gbps / 0.2 34h: 10.3125Gbps / 0.2	0.2 Gbps
800D	1	RO		Maximum Single Mode Optical Fiber		0Ah	0Ah: 10 km	1 km
800E	1	RO		Maximum Multi-Mode Optical Fiber		00h	00h: not supported	10 m
800F	1	RO		Maximum Copper Cable Length		00h	00h: not supported	1 m
8010	1	RO		Transmitter Spectral Characteristics 1		01h	00000001	N/A
			7	Reserved	0	0: Reserved	N/A	
			6		0	0: Reserved		
			5		0	0: Reserved		
			4	Number of Active Transmit Fibers	0	00001b: 1 Fiber	N/A	
			3		0			
			2		0			
			1		0			
0	1							

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit	
					Value	Hex			
Base ID Information									
8011	1	RO	7	Transmitter Spectral Characteristics 2	0	04h	00000100	N/A	
			6	Reserved	0		0: Reserved	N/A	
			5		0		0: Reserved	N/A	
			4		0		0: Reserved	N/A	
			3	Number of Wavelengths per active Transmit Fiber	0			00100b: 4 Wavelengths	N/A
			2		1				
			1		0				
			0		0				
8012	2	RO		Minimum Wavelength per Active Fiber		CAh	CA45h: 1294.53 nm	0.025 nm	
8013					45h				
8014	2	RO		Maximum Wavelength per Active Fiber		CCh	CCB8h: 1310.19 nm	0.025 nm	
8015					B8h				
8016	2	RO		Maximum per Lane Optical Width		08h	0834h: 2.1 nm	1 pm	
8017					34h				
8018	1	RO		Device Technology 1		21h	00100001	N/A	
			7	Laser Source Technology	0			0010b: DFB	N/A
			6		0				
			5		1				
			4		0				
			3	Transmitter modulation technology	0			0001b: EML	N/A
			2		0				
			1		0				
0	1								
8019	1	RO		Device Technology 2		44h	01000100	N/A	
			7	Wavelength control	0		0: No wavelength control	N/A	
			6	Cooled transmitter	1		1: Cooled or Semi-cooled transmitter device	N/A	
			5	Tunability	0		0: Transmitter NOT Tunable	N/A	
			4	VOA implemented	0		0: Detector side VOA NOT implement	N/A	
			3	Detector Type	0		01b: PIN Detector	N/A	
			2		1				
			1		CDR with EDC	0		0: CDR without EDC	N/A
0	Reserved	0		0: Reserved	N/A				
801A	1	RO		Signal Code		40h	01000000	N/A	
			7	Modulation	0		01b: NRZ	N/A	
			6		1				
			5	Signal coding	0		0000b: Non-PSK	N/A	
			4		0				
			3		0				
			2		0				
			1	Reserved	0		0: Reserved	N/A	
0	0		0: Reserved		N/A				
801B	1	RO		Maximum Total Optical Output Power per Connector		70h	11220.2uW	100 uW	
801C	1	RO		Maximum Optical Input Power per Network Lane		1Ch	2818.4uW	100 uW	
801D	1	RO		Maximum Power Consumption		50h	16000mW	200 mW	
801E	1	RO		Maximum Power Consumption in Low Power Mode		64h	2000mW	20 mW	
801F	1	RO		Maximum Operating Case Temp Range		46h	70degC	1 Dec	
8020	1	RO		Minimum Operating Case Temp Range		FBh	-5degC	1 degC	

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name	Bit Filed Name	Value		Description	LSB Unit
						Value	Hex		
Base ID Information									
8021	163h	RO		Vendor Name					ASCII
8022	75h								ASCII
8023	6Dh								ASCII
8024	69h								ASCII
8025	74h								ASCII
8026	6Fh								ASCII
8027	6Dh								ASCII
8028	6Fh								ASCII
8029	45h								ASCII
802A	6Ch								ASCII
802B	65h								ASCII
802C	63h								ASCII
802D	74h								ASCII
802E	72h								ASCII
802F	69h								ASCII
8030	63h								ASCII
8031	3	RO		Vendor OUI			00h	00005Fh	N/A
8034	16	RO	53h	Vendor Part Number	ASCII				
8035	43h								ASCII
8036	46h								ASCII
8037	31h								ASCII
8038	30h							1001: 100GE	ASCII
8039	31h							1011: OTU4/100GE	ASCII
803A	31h								ASCII
803B	4Ch								ASCII
803C	34h								ASCII
803D						L	4Ch	LN: LC, -5to70degC	ASCII
803E						N	4Eh	CN: SC, -5to70degC AN; Angled-LC, -5to70degC	ASCII
803F						G	47h		ASCII
8040						G	47h		ASCII
8041						0	30h		ASCII
8042						1	31h		ASCII
8043							20h		ASCII
8044	16	RO		Vendor Serial Number		\$	24h	Manufacturer serial number in ASCII code	ASCII
8054	8	RO		Date Code		\$	24h	Date code in YYYYMMDD	ASCII
805C	2	RO		Lot Code		\$	24h	Lot code in ASCII code.	ASCII
805D						\$	24h		ASCII
805E	10	RO		CLEI Code			20h	' in ASCII code.	ASCII
805F							20h		ASCII
8060							20h		ASCII
8061							20h		ASCII
8062							20h		ASCII
8063							20h		ASCII
8064							20h		ASCII
8065							20h		ASCII
8066							20h		ASCII
8067							20h		ASCII
8068	1	RO		CFP MSA Hardware Specification Revision Number			0Eh	Rev. 1.4	N/A
8069	1	RO		CFP MSA Management Interface Specification Revision Number			0Eh	Rev. 1.4	N/A
806A	2	RO		Module Hardware Version Number			01h	Version 1.0	N/A
806B							00h	(0.1: DS, 0.2: ES, 1.0 and higher: CS)	
806C	2	RO		Module Firmware Version Number			01h	Version 1.0	N/A
806D							00h	(0.1: DS, 0.2: ES, 1.0 and higher: CS)	

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
806E	1	RO	7	Digital Diagnostic Monitoring Type		0Ch	00001100	N/A
			6	Reserved	0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A
			3		Received power measurement type	1		1: Averaged Power
			2	Transmitted power measurement type	1		1: Averaged Power	N/A
			1	Reserved	0		0: Reserved	N/A
			0		0		0: Reserved	N/A
806F	1	RO		DDM Capability 1		03h	00000011	N/A
			7	Transceiver auxiliary monitor 2	0		00b: Not supported	N/A
			6		0		00b: Not supported	N/A
			5	Transceiver auxiliary monitor 1	0		00b: Not supported	N/A
			4		0		00b: Not supported	N/A
			3	Reserved	0		0: Reserved	N/A
			2	Transceiver SOA Ibias monitor	0		0: Not supported	N/A
			1	Transceiver Supply voltage monitor	1		1: Supported	N/A
			0	Transceiver temperature monitor	1		1: Supported	N/A
8070	1	RO		DDM Capability 2 (per Lane)		0Fh	00001111	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A
			3	Network Lane received power monitor	1		1: Supported	N/A
			2	Network Lane laser output power	1		1: Supported	N/A
			1	Network Lane laser bias current	1		1: Supported	N/A
			0	Network Lane laser temperature	1		1: Supported	N/A
8071	1	RO		Module Enhanced Options		E8h	11101000	
			7	Host Lane Loop-back	1		1: Supported	N/A
			6	Host Lane PRBS Supported	1		1: Supported	N/A
			5	Host Lane emphasis control	1		1: Supported	N/A
			4	Network Lane Loop-back	0		0: Not supported	N/A
			3	Network Lane PRBS	1		1: Supported	N/A
			2	Decision Threshold Voltage control	0		0: Not supported	N/A
			1	Decision Phase control functions	0		0: Not supported	N/A
			0	Unidirectional TX/RX only Operation	0		0: Not supported	N/A
8072	1	RO		Maximum High-Power-up Time		0Ah	0Ah: 10 sec.	1 sec
8073	1	RO		Maximum TX-Turn-on Time		01h	01h: 1 sec.	1 sec
8074	1	RO		Host Lane Signal Spec		01h	01h: CAUI	N/A
8075	1	RO		Heat Sink Type		00h	00000000	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A
			3		0		0: Reserved	N/A
			2		0		0: Reserved	N/A
			1		0		0: Reserved	N/A
0	Heat Sink Type	0		0: Flat Top	N/A			
8076	1	RO		Maximum TX-Turn-off Time		96h	96h: 150 ms	1ms
8077	1	RO		Maximum High-Power-down Time		01h	01h: 1 sec.	1sec

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
8078	1	RO		Module Enhanced Options 2		0Fh	00001111	
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4	Active Decision Voltage and Phase Function	0		0: Not supported	N/A
			3	RX FIFO Reset	1		1: Supported	N/A
			2	RX FIFO Auto Reset	1		1: Supported	N/A
			1	TX FIFO Reset	1		1: Supported	N/A
0	TX FIFO Auto Reset	1		1: Supported	N/A			
8079	1	RO		Transmitter Monitor Clock Options		05h	00000101	
			7	1/16 of Host Lane Rate	0		0: Not supported	N/A
			6	1/16 of Network Lane Rate	0		0: Not supported	N/A
			5	1/64 of Host Lane Rate	0		0: Not supported	N/A
			4	1/64 of Network Lane Rate	0		0: Not supported	N/A
			3	Reserved	0		0: Reserved	N/A
			2	1/8 of Network Lane Rate	1		1: Supported	N/A
			1	Reserved	0		0: Reserved	N/A
0	Monitor Clock Option	1		1: Supported	N/A			
807A	1	RO		Receiver Monitor Clock Options		05h	00000101	
			7	1/16 of Host Lane Rate	0		0: Not supported	N/A
			6	1/16 of Network Lane Rate	0		0: Not supported	N/A
			5	1/64 of Host Lane Rate	0		0: Not supported	N/A
			4	1/64 of Network Lane Rate	0		0: Not supported	N/A
			3	Reserved	0		0: Reserved	N/A
			2	1/8 of Network Lane Rate	1		1: Supported	N/A
			1	Reserved	0		0: Reserved	N/A
0	Monitor Clock Option	1		1: Supported	N/A			
807B	1	RO		Reserved		00h	0: Reserved	N/A
807C	1	RO		Reserved		00h	0: Reserved	N/A
807D	1	RO		Reserved		00h	0: Reserved	N/A
807E	1	RO		Reserved		00h	0: Reserved	N/A
807F	1	RO		CFP NVR 1 Checksum	0	24h	The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.	N/A

Table 8.2.2. CFP NVR-2

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Alarm/Warning Threshold Registers								
8080	2	RO		Transceiver Temp High Alarm	50h	80 degC	1/256 degC	
8081				Threshold	00h			
8082	2	RO		Transceiver Temp High Warning	4Bh	75 degC		
8083				Threshold	00h			
8084	2	RO		Transceiver Temp Low Warning	F6h	-10 degC		
8085				Threshold	00h			
8086	2	RO		Transceiver Temp Low Alarm	F1h	-15 degC		
8087				Threshold	00h			
8088	2	RO		VCC High Alarm Threshold	94h	3.795V		0.1 mV
8089				Threshold	3Eh			
808A	2	RO		VCC High Warning Threshold	8Dh	3.63V		
808B				Threshold	CCh			
808C	2	RO		VCC Low Warning Threshold	74h	2.97V		
808D				Threshold	04h			
808E	2	RO		VCC Low Alarm Threshold	6Dh	2.805V		
808F				Threshold	92h			
80A8	2	RO		Laser Bias Current High Alarm	D6h	110 mA	2uA	
80A9				Threshold	D8h			
80AA	2	RO		Laser Bias Current High Warning	C3h	100 mA		
80AB				Threshold	50h			
80AC	2	RO		Laser Bias Current Low Warning	75h	60 mA		
80AD				Threshold	30h			
80AE	2	RO		Laser Bias Current Low Alarm	61h	50 mA		
80AF				Threshold	A8h			
80B0	2	RO		Laser Output Power High Alarm	DBh	7.5 dBm	0.1 uW	
80B1				Threshold	AAh			
80B2	2	RO		Laser Output Power High Warning	8Ah	5.5 dBm		
80B3				Threshold	99h			
80B4	2	RO		Laser Output Power Low Warning	0Bh	-5.3 dBm		
80B5				Threshold	87h			
80B6	2	RO		Laser Output Power Low Alarm	07h	-7.3 dBm		
80B7				Threshold	46h			
80B8	2	RO		Laser Temperature High Alarm	3Ch	60 degC	1/256 degC	
80B9				Threshold	00h			
80BA	2	RO		Laser Temperature High Warning	37h	55 degC		
80BB				Threshold	00h			
80BC	2	RO		Laser Temperature Low Warning	1Eh	30 degC		
80BD				Threshold	00h			
80BE	2	RO		Laser Temperature Low Alarm	19h	25 degC		
80BF				Threshold	00h			
80C0	2	RO		Receive Optical Power High Alarm	DBh	7.5 dBm	0.1 uW	
80C1				Threshold	AAh			
80C2	2	RO		Receive Optical Power High Warning	9Bh	6 dBm		
80C3				Threshold	82h			
80C4	2	RO		Receive Optical Power Low Warning	02h	-11.6 dBm		
80C5				Threshold	B3h			
80C6	2	RO		Receive Optical Power Low Alarm	01h	-13.6 dBm		
80C7				Threshold	B4h			
80C8	55	RO		Reserved	00h	0000h: Reserved	N/A	
80FF	1	RO		CFP NVR 2 Checksum	24h	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.	N/A	

Table 8.2.3. CFP NVR-3

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Network Lane BOL Measurements								
8100	2	RO		RX Sensitivity for network lanes 0		24h	Measured Value	0.01 dBm
8101						24h		
8102	2	RO		RX Sensitivity for network lanes 1		24h	Measured Value	
8103						24h		
8104	2	RO		RX Sensitivity for network lanes 2		24h	Measured Value	
8105						24h		
8106	2	RO		RX Sensitivity for network lanes 3		24h	Measured Value	
8107						24h		
8120	2	RO		TX Power for network lanes 0		24h	Measured Value	0.01 dBm
8121						24h		
8122	2	RO		TX Power for network lanes 1		24h	Measured Value	
8123						24h		
8124	2	RO		TX Power for network lanes 2		24h	Measured Value	
8125						24h		
8126	2	RO		TX Power for network lanes 3		24h	Measured Value	
8127						24h		
8140	2	RO		Measured ER for network lanes 0		24h	Measured Value	0.01 dBm
8141						24h		
8142	2	RO		Measured ER for network lanes 1		24h	Measured Value	
8143						24h		
8144	2	RO		Measured ER for network lanes 2		24h	Measured Value	
8145						24h		
8146	2	RO		Measured ER for network lanes 3		24h	Measured Value	
8147						24h		
8160	2	RO		Path Penalty for network lanes 0		00h	0.8 dB	0.01dB
8161						50h		
8162	2	RO		Path Penalty for network lanes 1		00h	0.8 dB	
8163						50h		
8164	2	RO		Path Penalty for network lanes 2		00h	0.8 dB	
8165						50h		
8166	2	RO		Path Penalty for network lanes 3		00h	0.8 dB	
8167						50h		

Table 8.2.4. CFP NVR-4

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
User data registers.								
8180	1	RO	7~0	CFP NVR 3 Checksum	\$	24h	The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh inclusive.	N/A
8181	127	RO	7~1	Reserved		00h	00h: Reserved	N/A

Table 8.2.5. CFP Module VR 1

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Init Value		Description	LSB Unit
					Value	Hex		
Module Command/Setup Registers								
A011	1			Network Lane TX Control		0201h	This control acts upon all the network lanes.	
		RO	15	Reserved	0			N/A
		RW	14	TX PRBS Generator Enable	0		0: Normal operation, 1: PRBS mode. (Optional)	N/A
		RW	13	TX PRBS Pattern 1	0		00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	N/A
		RW	12	TX PRBS Pattern 0	0			N/A
		RO	11	TX De-skew Enable	0		0:Normal, 1:Disable	N/A
		RW	10	TX FIFO Reset	0		0: Normal operation, 1: Reset (Optional)	N/A
		RW	9	TX FIFO Auto Reset	1		0: Not Auto Reset, 1: Auto Reset. (Optional).	N/A
		RW	8	TX Reset	0		0: Normal operation, 1: Reset.	N/A
		RW	7	TX MCLK Control	0		000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network	N/A
		RW	6	TX MCLK Control	0			N/A
		RW	5	TX MCLK Control	0			N/A
		RO	4	Reserved	0			N/A
		RW	3	TX Rate Select (10G lane rate)	0		000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7,	N/A
		RW	2	TX Rate Select (10G lane rate)	0		011b:OTU4=11.2,	N/A
		RW	1	TX Rate Select (10G lane rate)	0		100b-111b: Reserved.	N/A
		RO	0	TX Reference CLK Rate Select	1		0: 1/16, 1: 1/64.	N/A
A012	1			Network Lane RX Control		0201h	This control acts upon all the network lanes.	
		RO	15	Active DVT and Phase function	0		0: not active, 1: active. (Optional)	N/A
		RW	14	RX PRBS Checker Enable	0		0: Normal operation, 1: PRBS mode. (Optional)	N/A
		RW	13	RX PRBS Pattern 1	0		00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	N/A
		RW	12	RX PRBS Pattern 0	0			N/A
		RO	11	RX Lock RX_MCLK to Ref_CLK	0		0: Normal, 1: Lock RX_MCLK to REFCLK.	N/A
		RO	10	Network Lane Loop-back	0		0: Normal operation, 1: Network lane loop-back. (Optional)	N/A
		RW	9	RX FIFO Auto Reset	1		0: Not auto reset, 1: Auto reset. (Optional).	N/A
		RW	8	RX Reset	0		0: Normal operation, 1: Reset.	N/A
		RW	7	RX MCLK Control	0		000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane	N/A
		RW	6	RX MCLK Control	0			N/A
		RW	5	RX MCLK Control	0			N/A
		RW	4	RX FIFO Reset	0		0: Normal, 1: Reset. (Optional).	N/A
		RW	3	RX Rate Select	0		000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7,	N/A
		RW	2	RX Rate Select	0		011b:OT U4=11.2, 100b-111b: Reserved	N/A
		RW	1	RX Rate Select	0			N/A
		RO	0	RX Reference CLK Rate Select	1		0: 1/16, 1: 1/64.	N/A
A029	1			Module General Status Enable		A370h	1: Enable signal to assert GLB_ALRM . Bits 14-0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM . Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation. Figure 10	
		RW	15	GLB_ALRM Master Enable	1		1: Enable.	N/A
		RO	14	Reserved	0			N/A
		RW	13	HW Interlock	1		1: Enable.	N/A
		RO	12	Reserved	0			N/A
		RO	11	Reserved	0			N/A
		RO	10	Loss of REFCLK Input Enable	0		1: Enable.	N/A
		RW	9	TX_JITTER_PLL_LOL Enable	1		1: Enable.	N/A
		RW	8	TX_CMU_LOL Enable	1		1: Enable.	N/A
		RO	7	TX_LOSF Enable	0		1: Enable.	N/A
		RW	6	TX_HOST_LOL Enable	1		1: Enable.	N/A
		RW	5	RX_LOS Enable	1		1: Enable.	N/A
		RW	4	RX_NETWORK_LOL Enable	1		1: Enable.	N/A
		RO	3	Out of Alignment Enable	0		1: Enable.	N/A
		RO	2	Reserved	0			N/A
		RO	1	Reserved	0			N/A
		RO	0	Reserved	0			N/A

Table 8.2.6. Network Lane VR1

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Init Value		Description	LS B Unit
					Value	Hex		
Network Lane FAWS Registers								
A250	4			Network Lane n Fault and Status		001Ch	16 registers, one for each network lane, represent 16 Network lanes. n = 0, 1, ..., N-1. N_max = 16. Actual N is module dependent.	
		RO	15	Lane TEC Fault Enable	0		0: Disable, 1: Enable.	N/A
		RO	14	Lane Wavelength Unlocked Fault Enable	0		0: Disable, 1: Enable.	N/A
		RO	13	Lane APD Power Supply Fault Enable	0		0: Disable, 1: Enable.	N/A
		RO	12	Reserved	0			N/A
		RO	11	Reserved	0			N/A
		RO	10	Reserved	0			N/A
		RO	9	Reserved	0			N/A
		RO	8	Reserved	0			N/A
		RO	7	Lane TX_LOSF Enable	0		0: Disable, 1: Enable.	N/A
		RO	6	Lane TX_LOL Enable	0		0: Disable, 1: Enable.	N/A
		RO	5	Reserved	0			N/A
		RW	4	Lane RX_LOS Enable	1		0: Disable, 1: Enable.	N/A
		RW	3	Lane RX_LOL Enable	1		0: Disable, 1: Enable.	N/A
		RW	2	Lane RX_FIFO Status Enable	1		0: Disable, 1: Enable.	N/A
		RO	1	Reserved	0			N/A
		RO	0	Reserved	0			N/A

Table 8.2.7. Host Lane VR1

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Init Value		Description	LS B Unit
					Value	Hex		
Network Lane FAWS Registers								
A420	16			Host Lane m Fault and Status Enable		0001h	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, ..., M-1. M_max = 16. Actual M is module dependent.	
		RO	15-2	Reserved	0			N/A
		RW	1	Lane TX_FIFO Error Enable	0		1: Enable.	N/A
		RW	0	TX_HOST_LOL Enable	1		1: Enable.	N/A

8.3 Registers for Digital Diagnostic Monitors (DDM)

Table 8.3.1. CFP Module VR1 Module Analog A/D Registers

CFP Module VR1						
Hex Addr.	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to +127 255/256 degC. MSA valid range is between -40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h
A030	1	RO	15~0	Module Power supply 3.3 V Monitor A/D Value	Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 0.1 mV, yielding a total measurement range of 0 to 6.5535 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.	0000h

Table 8.3.2. Network Lane VR2 A/D value measurement Registers

Network Lane VR 2						
Hex Addr.	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
Network Lane A/D value Measurement Registers						
A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.	0000h
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Measured TX output power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a range of laser output power from 0 to 6.5535 mW (-40 to +8.2 dBm). Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	0000h
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to +127 255/256 degC. MSA valid range is between -40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. The accuracy shall be +/- 2dB when input average power is between -10.6dBm and +4.5dBm, over the specified operating temperature and voltage.	0000h

9. Qualification Testing

The CFP series 100Gb/s transceivers are qualified to internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

10. RoHS COMPLIANCY

Compliance versus requirements contained within the following reference document is guaranteed: 'DIRECTIVE 2011/65/EU OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast)'.

11. Laser Safety Information

The CFP series transceivers use a semiconductor laser that is classified as Class 1 laser products per the laser safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC60825-1:2007 and IEC60825-1:2001 International standards.